IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Andrew Pickering	Docket:	TID-32491
Serial No.:	TBD	Examiner:	TBD
Filed:	Herewith	Art Unit:	TBD
For:	PARALLEL DATA INTERFACE		

PRELIMINARY AMENDMENT

Assistant Commissioner For Patents

Washington, D. C. 20231

"EXPRESS MAIL" mailing label number EL360245065US, Date of Deposit: : **25 May 2001.** I hereby certify that the Preliminary Amendment and the accompanying Application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 § CFR 1.10 on the above-mentioned date and is addressed to the Assistant Commissioner of Patents, Box New Applications, Washington, DC 20231.

Allen B. Kroger

Sir:

Before examination of the above-identified patent application, please make the following amendments:

IN THE SPECIFICATION:

Replacement page 3 and the abstract are enclosed herewith. Replacement pages 10-13 are enclosed herewith so that the original claims will appear on separate pages.

IN THE CLAIMS:

Please amend claims 1-7, 9-11 as follows:

1. (Amended) Apparatus for receiving parallel transmitted data via plurality of channels comprising by means (30) to generate a clock signal (50) on the basis of the received data and means (40) associated with each of said channels to synchronise data received on the associated channel with the generated clock signal (50).

2. (Amended) Apparatus as claimed in claim 1 wherein the means (30) to generate a clock signal includes clock signal delay means (32) which delay the clock signal (50) by a predetermined amount with respect to a clock input derived from the received data.

3. (Amended) Apparatus as claimed in claim 2 wherein the predetermined amount is half a maximum delay (Td) available to each data channel.

4. (Amended) Apparatus as claimed in claim 1 wherein the synchronising means (40) each include variable delay means (42) for applying a variable delay to each of the channels.

5. (Amended) Apparatus as claimed in claim 4 wherein each variable delay means (42) is incremented over a range of available delays (0-Td) and is controlled to revert to its maximum delay in the event that the maximum delay (Td) is insufficient to achieve synchronisation, or to its maximum delay (Td) if its maximum delay is insufficient to achieve synchronisation.

6. (Amended) Apparatus as claimed in claim 4 wherein the variable delay means (42) include means (104) for mixing a non-delayed signal with a maximally delayed signal in variable proportions to output a variable delay signal.

7. (Amended) Apparatus as claimed in claim 6 wherein said mixing means includes a plurality of delay stages (112).

9. (Amended) A method as claimed in claim 8 wherein the clock signal (50) is delayed by a predetermined amount with respect to a clock input derived from said received data .

10. (Amended) A method as claimed on claim 9 wherein said predetermined amount is half maximum delay (Td) available to each data channel.

11. (Amended) A method as claimed in claim 8 wherein a variable delay on each of the channels is incremented over a range of available delays (0-Td) and in which the delay is controlled to revert to its minimum in the event that the maximum delay is insufficient to achieve synchronisation and vice versa.

Please add claims 12-16 as follows:

--12. (New) Apparatus as claimed in claim 2 wherein the synchronising means (40) each include variable delay means (42) for applying a variable delay to each of the channels.

13. (New) Apparatus as claimed in claim 3 wherein the synchronising means (40) each include variable delay means (42) for applying a variable delay to each of the channels.

14. (New) Apparatus as claimed in claim 5 wherein the variable delay means (42) include means (104) for mixing a non-delayed signal with a maximally delayed signal in variable proportions to output a variable delay signal.

15. (New) A method as claimed in claim 9 wherein a variable delay on each of the channels is incremented over a range of available delays (0-Td) and in which the delay is controlled to revert to its minimum in the event that the maximum delay is insufficient to achieve synchronisation and vice versa.

16. (New) A method as claimed in claim 10 wherein a variable delay on each of the channels is incremented over a range of available delays (0-Td) and in which the delay is controlled to revert to its minimum in the event that the maximum delay is insufficient to achieve synchronisation and vice versa.--

REMARKS

Entry and favorable action of the claims are earnestly solicited in light of the above amendments.

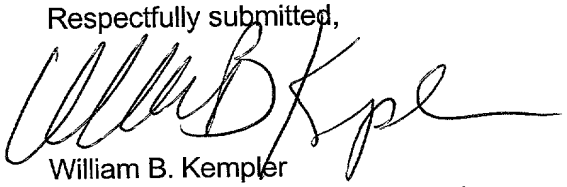
Applicants have amended the claims inter alia to avoid multiple dependent claims and to place the claims in the appropriate form.

Early action on the merits is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current preliminary amendment. The attached page is captioned **"Version with markings to show changes made."**

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

SUMMARY OF THE INVENTION

[The] One aspect of the present invention provides apparatus for receiving parallel transmitted data in a plurality of channels comprising means to generate a clock signal on the basis of the received data and means associated with each of said channels to synchronise data received on the associated channel with the generated clock.

IN THE CLAIMS:

1. (Amended) Apparatus for receiving parallel transmitted data via plurality of channels [characterised by] comprising means (30) to generate a clock signal (50) on the basis of the received data and means (40) associated with each of said channels to [synchronise] synchronize data received on the associated channel with the generated clock signal (50).

2. (Amended) Apparatus as claimed in claim 1 [in which] wherein the means (30) to generate a clock signal includes clock signal delay means (32) which delay the clock signal (50) by a predetermined amount with respect to a clock input derived from the received data.

3. (Amended) Apparatus as claimed in claim 2 [in which] wherein the predetermined amount is half a maximum delay (Td) available to each data channel.

4. (Amended) Apparatus as claimed in claim 1[, 2 or 3 in which] wherein the [synchronising] synchronizing means (40) each include variable delay means (42) for applying a variable delay to each of the channels.

5. (Amended) Apparatus as claimed in claim 4 [in which] wherein each variable delay means (42) is incremented over a range of available delays (0-Td) and is controlled to revert to its maximum delay in the event that the maximum delay (Td) is insufficient to achieve [synchronisation] synchronization, or to its maximum delay (Td) if its maximum delay is insufficient to achieve [synchronisation] synchronization.

6. (Amended) Apparatus as claimed in claim 4 [or 5 in which] wherein the variable delay means (42) include means (104) for mixing a non-delayed signal with a maximally delayed signal in variable proportions to output a variable delay signal.

7. (Amended) Apparatus as claimed in claim 6 [in which] wherein said mixing means includes a plurality of delay stages (112).

9. (Amended) A method as claimed in claim 8 [in which] wherein the clock signal (50) is delayed by a predetermined amount with respect to a clock input derived from said received data .

10. (Amended) A method as claimed on claim 9 [in which] wherein said predetermined amount is half maximum delay (Td) available to each data channel.

11. (Amended) A method as claimed in claim 8[, 9 or 10 in which] wherein a variable delay on each of the channels is incremented over a range of available delays (0-Td) and in which the delay is controlled to revert to its minimum in the

event that the maximum delay is insufficient to achieve [synchronisation] synchronization and vice versa.

Please add claims 12-16 as follows:

--12. (New) Apparatus as claimed in claim 2 wherein the synchronizing means (40) each include variable delay means (42) for applying a variable delay to each of the channels.

13. (New) Apparatus as claimed in claim 3 wherein the synchronizing means (40) each include variable delay means (42) for applying a variable delay to each of the channels.

14. (New) Apparatus as claimed in claim 5 wherein the variable delay means (42) include means (104) for mixing a non-delayed signal with a maximally delayed signal in variable proportions to output a variable delay signal.

15. (New) A method as claimed in claim 9 wherein a variable delay on each of the channels is incremented over a range of available delays (0-Td) and in which the delay is controlled to revert to its minimum in the event that the maximum delay is insufficient to achieve synchronization and vice versa.

16. (New) A method as claimed in claim 10 wherein a variable delay on each of the channels is incremented over a range of available delays (0-Td) and in which the delay is controlled to revert to its minimum in the event that the maximum delay is insufficient to achieve synchronization and vice versa.--

Parallel Data Interface

Abstract

Parallel transmitted data in a plurality of channels is [synchronised] synchronized by generating a clock on the basis of the received data and [synchronising] synchronizing the data received on each channel with the generated clock signal (50).

skew in the parallel transmission channel have a significant effect in the ability to recover received data.

One approach would be to regenerate a separate data recovery clock for each of the parallel channels. This is however impractical for a large number of parallel data channels, and also does not deal with the lack of synchronisation between the data channels.

SUMMARY OF THE INVENTION

One aspect of the present invention provides apparatus for receiving parallel transmitted data in a plurality of channels comprising means to generate a clock signal on the basis of the received data and means associated with each of said channels to synchronise data received on the associated channel with the generated clock.

In this arrangement a single clock signal is generated which is used for all the data channels. This means that the apparatus is easily scaleable to receive data from large numbers of parallel channels.

In synchronising all the data channels with a single clock the apparatus also removes the skew between the data channels. Thus the apparatus can simply present as-received but re-aligned data signals for subsequent processing. Alternatively the apparatus can perform the data recovery at the same time as re-aligning the channels. The clock signal may be generated on the basis of a single received channel. That channel may be a channel designated for the transmission of a clock signal

Claims

1. Apparatus for receiving parallel transmitted data via plurality of channels comprising means (30) to generate a clock signal (50) on the basis of the received data and means (40) associated with each of said channels to synchronize data received on the associated channel with the generated clock signal (50).

2. Apparatus as claimed in claim 1 wherein the means (30) to generate a clock signal includes clock signal delay means (32) which delay the clock signal (50) by a predetermined amount with respect to a clock input derived from the received data.

3. Apparatus as claimed in claim 2 wherein the predetermined amount is half a maximum delay (Td) available to each data channel.

4. Apparatus as claimed in claim 1 wherein the synchronizing means (40) each include variable delay means (42) for applying a variable delay to each of the channels.

5. Apparatus as claimed in claim 4 wherein each variable delay means (42) is incremented over a range of available delays (0-Td) and is controlled to revert to its maximum delay in the event that the maximum delay (Td) is insufficient to achieve synchronization, or to its maximum delay (Td) if its maximum delay is insufficient to achieve synchronization.

6. Apparatus as claimed in claim 4 wherein the variable delay means (42) include means (104) for mixing a non-delayed signal with a maximally delayed signal in variable proportions to output a variable delay signal.

7. Apparatus as claimed in claim 6 wherein said mixing means includes a plurality of delay stages (112).

8. A method of synchronizing data signals received via a plurality of channels comprising the steps of:

generating a clock signal (50) on the basis of the received data; and

synchronizing data received on each channel with the generated clock signal (50).

9. A method as claimed in claim 8 wherein the clock signal (50) is delayed by a predetermined amount with respect to a clock input derived from said received data .

10. A method as claimed on claim 9 wherein said predetermined amount is half maximum delay (Td) available to each data channel.

11. A method as claimed in claim 8 wherein a variable delay on each of the channels is incremented over a range of available delays (0-Td) and in which the delay is controlled to revert to its minimum in the event that the maximum delay is insufficient to achieve synchronization and vice versa.

Parallel Data Interface

Abstract

Parallel transmitted data in a plurality of channels is synchronized by generating a clock on the basis of the received data and synchronizing the data received on each channel with the generated clock signal (50).